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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,300	10/15/2003	Andrew Martin Mallinson	ESST-02501	7923

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/687,300	MALLINSON, ANDREW MARTIN
	Examiner	**Art Unit**
	Jean B Jeanglaude	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,7 and 11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7 and 11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 12 - 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Setty et al. (US Patent Number 5,877,720).

3. Regarding claims 1, 12, Setty et al. discloses an analog-to-digital converter and method (fig. 1) comprising: a converter input for receiving an analog input signal to be converted (the input of the comparators 19a,...,19c where V_{in} is applied); an input impedance network (resistor string shown in fig. 1) for creating a plurality of reference signals ((V_{REF} , fig. 1) ; a plurality of comparators 19a,...,19c, fig. 1) corresponding to the plurality of reference signals [as noted another input of the comparators is coupled to the tap voltages as shown in fig. 1], each of the comparators having a first comparator input connected to the input impedance network to provide the comparator with one of the plurality of reference signals [as noted another input of the comparators is coupled to the tap voltages as shown in fig. 1], a second comparator input connected to the impedance network for receiving the analog input signal [one of the input of the comparators is coupled to the input V_{in}), a third comparator input connected to its own enabling signal source for receiving an enabling signal [the inputs of the comparators are used to control the operation of the latch clock (13, 22, fig. 1) to receive an enable signal] [see fig. 1], and a comparator output (col 5, lines 60 - 67) that outputs a signal

only when signals are received at the same time at the first, second, and third comparator inputs wherein the transfer characteristic of the output of each comparator is substantially linear within a region [it is inherent that the output of each comparator is substantially linear with a region based on the fact that if the input voltage produces a digital output which is equal to 1 based on the assumption in col 5, lines 59 - 62, the output signal is equal to one (1) for a certain period of time, thereby the output of the comparator is linear for that incremental of time. When the input voltage produces a digital output that is equal to zero (0) based on the assumption in col 5, lines 62 - 64, the output signal is equal to zero (0) for a certain period of time, thereby the output of the comparator is linear for that incremental of time], and a converter output connected to a comparator output of each of the plurality of comparators (fig. 1).

4. Regarding claim 2, Setty et al. discloses an analog-to-digital converter (fig. 1), wherein the first comparator input and second comparator input of each of the plurality of comparators control the transfer of an enabling signal at the third comparator input to a signal at the comparator output, and wherein the transfer characteristic of each comparator between the third comparator input to the comparator output is substantially linear [the inputs of the comparators are used to control the operation of the latch clock (13, 22, fig. 1) to receive an enable signal], thereby Setty et al. discloses an analog-to-digital converter, wherein the first comparator input and second comparator input of each of the plurality of comparators control the transfer of an enabling signal at the third comparator input to a signal at the comparator output, and wherein the transfer

characteristic of each comparator between the third comparator input to the comparator output is substantially linear.

5. Regarding claims 11, 14, Setty et al. discloses an analog-to-digital converter (fig. 1) wherein the analog input signal is a differential signal applied across the impedance network [the analog input as shown in Setty et al. is differential across the resistor string].

6. Regarding claim 13, Setty et al. Discloses a method (fig. 1) comprises a latch that creates a virtual comparator during an iteration of the repeated comparisons in a successive approximation manner by enabling more than one of said plurality of comparators at the same time and modifying the outputs of the enabled comparators prior to summing the outputs together, such modifications in proportions that linearly interpolate between the outputs of the enabled comparators so as to simulate a virtual comparator having an interstitial output between the outputs of the enabled comparators (col 6, lines 25 – 44).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6, 7, 11, 15 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Setty et al. in view of Mangelsdorf et al. (US Patent Number 4,596,976).

9. Regarding claim 6, Setty et al. discloses an analog-to-digital converter (fig. 1) comprising: a converter input for receiving an analog input signal to be converted (the input of the comparators 19a,...,19c where V_{in} is applied); an input impedance network (resistor string shown in fig. 1) for creating a plurality of reference signals (V_{REF} , fig. 1) ; a plurality of comparators (19a,...,19c, fig. 1) corresponding to the plurality of reference signals [as noted another input of the comparators is coupled to the tap voltages as shown in fig. 1], each of the comparators having a first comparator input connected to the input impedance network to provide the comparator with one of the plurality of reference signals [as noted another input of the comparators is coupled to the tap voltages as shown in fig. 1], a second comparator input connected to the input impedance network to provide the comparator with a different one of the plurality of reference signals (fig. 1) [as noted another input of the comparators is coupled to the tap voltages as shown in fig. 1], a third comparator input connected to its own enabling signal source for receiving an enabling signal, and a comparator output that outputs a signal only when signals are received at the same time at the first, second, and third comparator inputs [the inputs of the comparators are used to control the operation of the latch clock (13, 22, fig. 1) to receive an enable signal], and a converter output connected to a comparator output of each of said plurality of comparators and configured to output a signal having linear characteristics within a region [it is inherent that the output of each comparator is substantially linear with a region based on the fact that if the input voltage produces a digital output which is equal to 1 based on the assumption in col 5, lines 59 - 62, the output signal is equal to one (1) for a certain

period of time, thereby the output of the comparator is linear for that incremental of time. When the input voltage produces a digital output that is equal to zero (0) based on the assumption in col 5, lines 62 - 64, the output signal is equal to zero (0) for a certain period of time, thereby the output of the comparator is linear for that incremental of time] (fig. 1). Setty et al. fail to disclose the analog-to-digital converter that comprises an input impedance network connected to the input converter for creating a plurality of reference signals having a parabolic profile. However, Mangelsdorf et al., in the same field of endeavor, discloses an integrated circuit analog-to-digital converter (fig. 15) that utilizes both transistors and array of transistors to create parabolic voltage distribution (abstract; col 3, lines 39 – 57; col 4, lines 40 – 44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Setty et al.'s system with that of Mangelsdorf et al. in order to provide a high speed analog-to-digital converter.

10. Regarding claim 15, Setty et al. discloses an analog to digital converter (fig. 1) comprising a converter input for receiving an analog input signal to be converted to digital data (the input of the comparators 19a,...,19c where V_{in} is applied) ; a network including a bank of resistors (14a,..., 14c); a plurality of comparators (19a,...,19c, fig. 1) corresponding to the plurality reference signals (V_{REF}), each comparator (19a,...19c, fig. 1) includes an enablement signal input connected to an enabling signal source for receiving an enabling signal [the inputs of the comparators are used to control the operation of the latch clock (13, 22, fig. 1) to receive an enable signal] [see fig. 1], and a comparator output (col 5, lines 60 - 67) that outputs a signal when the comparator is

enabled; and a converter output connected to a common output of each of the plurality of comparators, wherein the output is configured to output a value that is interpolated between two nodes to create a virtual comparator occurring between two nodes wherein the converter output is configured to output a signal that is linear with a region [it is inherent that the output of each comparator is substantially linear with a region based on the fact that if the input voltage produces a digital output which is equal to 1 based on the assumption in col 5, lines 59 - 62, the output signal is equal to one (1) for a certain period of time, thereby the output of the comparator is linear for that incremental of time. When the input voltage produces a digital output that is equal to zero (0) based on the assumption in col 5, lines 62 - 64, the output signal is equal to zero (0) for a certain period of time, thereby the output of the comparator is linear for that incremental of time] (fig. 1). Setty et al. fails to discloses an analog-to-digital converter wherein a plurality of nodes occurring between each resistor a plurality of current sources, where each current source corresponds to each node wherein each resistor and corresponding current source is configured to create an individual voltage reference having a value that occurs in a parabolic manner in relation to other voltage reference's occurring across the impedance network wherein the parabolic impedance network provides parabolic reference voltage inputs summed together with an input voltage to an input of each corresponding comparator. However, Mangelsdorf et al., in the same field of endeavor, discloses an integrated circuit analog-to-digital converter (fig. 15) that utilizes both transistors and array of transistors to create parabolic voltage distribution (abstract; col 3, lines 39 – 57; col 4, lines 40 – 44). The analog-to-digital system

discloses in Mangelsdorf et al. (fig. 1) comprises a resistor string (see fig. 15) in which a current source is located at each node of each resistor (see fig. 15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Setty et al.'s system with that of Mangelsdorf et al. in order to provide a high speed analog-to-digital converter.

11. Regarding claim 7, Setty et al. discloses an analog-to-digital converter (fig. 1), wherein the first comparator input and second comparator input of each of the plurality of comparators control the transfer of an enabling signal at the third comparator input to a signal at the comparator output, and wherein the transfer characteristic of each comparator between the third comparator input to the comparator output is linear [the inputs of the comparators are used to control the operation of the latch clock (13, 22, fig. 1) to receive an enable signal], thereby Setty et al. discloses an analog-to-digital converter (fig. 1), wherein the first comparator input and second comparator input of each of the plurality of comparators control the transfer of an enabling signal at the third comparator input to a signal at the comparator output, and wherein the transfer characteristic of each comparator between the third comparator input to the comparator output is linear.

12. Regarding claim 16, Setty et al. discloses an analog to digital converter (fig. 1) wherein the converter output connected to a common output of each of the plurality of comparators is configured to output a value that is interpolated between two nodes according to the formula $V_{iout} = K_i. E_i$, where $N \geq i \geq 1$ Vi is the difference between the input signal applied to comparator Ci, and Ei is the value of an enabling signal that can

be varied between two consecutive integers to create a virtual comparator occurring between two nodes and wherein the output comparator is substantially linear with a region [it is inherent that the output of each comparator is substantially linear with a region based on the fact that if the input voltage produces a digital output which is equal to 1 based on the assumption in col 5, lines 59 - 62, the output signal is equal to one (1) for a certain period of time, thereby the output of the comparator is linear for that incremental of time. When the input voltage produces a digital output that is equal to zero (0) based on the assumption in col 5, lines 62 - 64, the output signal is equal to zero (0) for a certain period of time, thereby the output of the comparator is linear for that incremental of time] (col 5, lines 59 – 64; col 6, lines 25 – 44).

13. Regarding claim 17 - 19, the combination of Setty et al. and Mangelsdorf would achieve the same end result as an analog-to-digital converter wherein the parabolic impedance network is configured to provide a reference voltage to the input of a comparator of each of the plurality of comparators in a manner that would produce reference voltages in a parabolic manner, where the reference voltage provided to one comparator is of a relatively lower value than the reference voltage provided to an intermediately located comparator, and where the reference voltage of the intermediately located comparator receives a maximum voltage value relative to the other comparators; as an analog-to-converter wherein the parabolic impedance network is configured to provide a reference voltage to the input of a comparator of each of the plurality of comparators in a manner that would produce reference voltages in a parabolic manner, where the reference voltage provided to one comparator is of a

relatively higher value than the reference voltage provided to an intermediately located comparator, and where the reference voltage of the intermediately located comparator receives a minimum voltage value relative to the other comparators and as an analog-to-digital converter wherein the comparators each include a pair of transistors, wherein the parabolic impedance network is configured to provide a reference voltage to the drain of one of a pair of transistors of each of the plurality of comparators in a manner that would produce reference voltages in a parabolic manner, where the reference voltage provided to one comparator is of a relatively higher value than the reference voltage provided to an intermediate comparator, and where the intermediate comparator receives of a minimum voltage value relative to the other comparators **since** Mangelsdorf et al. discloses a system that comprises an impedance network that provides a parabolic voltage distribution along its path. In doing so Mangelsdorf et al.'s system would supply relatively lower and higher voltages to Setty's comparators when combined with Setty et al.'s system. Moreover, Mangelsdorf et al. discloses a system that adjusts the parabolic peak which allows minimum voltage to particular comparators (fig. 15; col 3, lines 35 57).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude

Jean Bruner Jeanglaude
Primary Examiner
October 14, 2004